WHAT IS CLAIMED IS:

1. A method for manufacturing semiconductor chip that a semiconductor wafer, having a surface segmented by streets and formed with a plurality of circuits, is divided into individual circuit-based semiconductor chips, the method comprising:

a support substrate integration step of bonding a surface of a semiconductor wafer to a light-transmissive support substrate through an adhesive layer having an adhesion force to reduce upon exposed to light radiation, thereby exposing a back surface of the semiconductor wafer;

a grinding step of resting the semiconductor wafer integrated with the support substrate on a chuck table of a grinding device and grinding a back surface of the semiconductor wafer;

a tape bonding step of bonding a tape on the back surface of the semiconductor wafer integrated with the support substrate after the grinding step, while bonding a frame on a periphery of the tape;

a re-bonding step of applying light radiation to the adhesive layer from a side of the support substrate before or after the tape bonding step to thereby reduce the adhesion force of the adhesive layer, and removing the support substrate and adhesive layer from the surface of the semiconductor wafer after the tape bonding step to thereby support the semiconductor wafer by the tape and a frame; and

a dicing step of resting the semiconductor wafer supported by the tape and frame on a chuck table of a dicing apparatus and cutting along the streets segmenting for a plurality of circuits into individual semiconductor chips.

2. A method for manufacturing semiconductor chip that a semiconductor wafer, having a surface segmented by streets and formed with a plurality of circuits, is divided into individual circuit-based semiconductor chips, the method comprising:

a groove forming step of resting a semiconductor wafer on a chuck table of a dicing apparatus and forming grooves on street surface segmenting for a plurality of circuits;

a support substrate integrating step of bonding a surface of the semiconductor wafer to a light-transmissive support substrate through an adhesive layer having an adhesion force to reduce upon exposed to light radiation, thereby

exposing a back surface of the semiconductor wafer;

a grinding step of resting the semiconductor wafer integrated with the support substrate on a chuck table of a grinding apparatus and grinding the back surface of the semiconductor wafer into individual semiconductor chips until the grooves are surfaced;

a tape bonding step of bonding a tape on the back surface of the semiconductor chip in a state integrated with the support substrate of after grinding step and maintaining an outer shape of the semiconductor wafer, and supporting a periphery of the tape by a frame; and

a re-bonding step of applying light radiation to the adhesive layer at a side close to the support substrate before or after the tape bonding step to thereby reduce an adhesion force of the adhesive layer, and removing the supporting substrate and adhesive layer from the surface of the semiconductor wafer after the tape bonding step thereby supporting the semiconductor wafer by the tape and frame.

3. A method for manufacturing semiconductor chip that a semiconductor wafer, having a surface segmented by streets and formed with a plurality of circuits, is divided into individual circuit-based semiconductor chips, the method comprising:

a groove forming step of resting a semiconductor wafer on a chuck table of a dicing apparatus and forming grooves on street surface segmenting for a plurality of circuits;

a support substrate integrating step of bonding a surface of the semiconductor wafer to a light-transmissive support substrate through an adhesive layer having an adhesion force to reduce upon exposed to light radiation, thereby exposing a back surface of the semiconductor wafer;

a grinding step of resting the semiconductor wafer integrated with the support substrate on a chuck table of a grinding apparatus and grinding the back surface of the semiconductor wafer into individual semiconductor chips until the grooves are surfaced; and

a semiconductor chip detaching step of applying light radiation to the adhesive layer at a side close to the support substrate to thereby reduce an adhesion force thereof, and removing semiconductor chips from the support substrate and adhesive layer.

4. A method according to claim 1, 2 or 3, wherein the support substrate integrating step is carried out using the support substrate having an outer shape greater than an outer shape of the semiconductor wafer, the grinding step being carried out while measuring a thickness of the semiconductor wafer by contacting probes of a thickness measuring instrument respectively with a grinding surface of the semiconductor wafer and with a surface of the support substrate.

5. A method according to claim 1, wherein the adhesive layer is a liquid resin, the liquid resin being formed of a composition of quinone-diazido compound and resin to foam and reduce in adhesion force upon exposed to ultraviolet radiation, wherein the liquid resin is coated on the surface of the support substrate or the semiconductor wafer.

6. A method according to claim 2, wherein the adhesive layer is a liquid resin, the liquid resin being formed of a composition of quinone-diazido compound and resin to foam and reduce in adhesion force upon exposed to ultraviolet radiation, wherein the liquid resin is coated on the surface of the support substrate or the semiconductor wafer.

7. A method according to claim 3, wherein the adhesive layer is a liquid resin, the liquid resin being formed of a composition of quinone-diazido compound and resin to foam and reduce in adhesion force upon exposed to ultraviolet radiation, wherein the liquid resin is coated on the surface of the support substrate or the semiconductor wafer.

8. A method according to claim 5, 6 or 7, wherein the quinone-diazido compound is quinone-diazido sulphonic acid ester obtained by reacting polyhydroxy benzophenone, such as tri- or tetra-hydroxy benzophenone, with 1,2-naphtoquinone diazido-5-sulphonic acid, 1,2-naphtoquinone diazido-4-sulphonic acid, or sulphonic acid chloride thereof or the like, or at least one of sulphonic oxide compound selected from 1,2-quinone-diazido sulphonic acid or sulphonic acid chloride thereof or the like.

9. A method according to claim 5, wherein the resin is at least one resin

selected from acryl, urethane, polyester, novolak phenol and a derivative thereof, polyvinyl phenol and a derivative thereof, and silicone and a derivative thereof, the resin being introduced with polymeric unsaturated radical.

10. A method according to claim 6, wherein the resin is at least one resin selected from acryl, urethane, polyester, novolak phenol and a derivative thereof, polyvinyl phenol and a derivative thereof, and silicone and a derivative thereof, the resin being introduced with polymeric unsaturated radical.

11. A method according to claim 7, wherein the resin is at least one resin selected from acryl, urethane, polyester, novolak phenol and a derivative thereof, polyvinyl phenol and a derivative thereof, and silicone and a derivative thereof, the resin being introduced with polymeric unsaturated radical.

12. A method according to claim 9, 10 or 11, wherein the liquid resin has a viscosity of 10 - 100000 mPa · s.

13. A method according to claim 5, 6 or 7, wherein, in the support substrate integrating step, the liquid resin is dripped on the surface of the support substrate or the semiconductor wafer and spin-coated under rotation at 100 - 8000 rpm for 5 seconds or more, and thereafter the semiconductor wafer and the support substrate are united together through the liquid resin and baked at 50 - 150 °C for 30 seconds to 20 minutes.

14. A method according to any of claim 1, 2 or 3, wherein the support substrate is formed by a transparent plate of glass or plastic having a thickness of 0.5 - 2.5 mm.